What is claimed is:

1. A filter coefficient design method in a digital filter having a plurality of filter coefficients that are expressed with CSD code words of n bits (n: natural number more than 2), comprising the step of: making code word subexpression for random filter coefficients out of the filter coefficients as a virtual common subexpression that is relevant to a predetermined common subexpression so that adders are shared with the common subexpression in tap lines of the random filter coefficients.

2. The method of claim 1, wherein the virtual common subexpression becomes identical to the common subexpression through bit-shift.

3. The method of claim 1, wherein the virtual common subexpression becomes identical to the common subexpression through bit-add.

4. The method of claim 1, wherein the virtual common subexpression becomes identical to the common subexpression through bit-inversion.

5. The method of claim 1, wherein the virtual common subexpression becomes identical to the common subexpression through at least two more processes out of bit-shift, bit-add and bit-inversion.

6. The method of claim 1, wherein the digital filter is a linear phase FIR filter.

7. A method for receiving and filtering input signals of digital samples of k bits (k: natural numbers more than 4) in a digital filter having filter characteristics that are created by filter coefficients being expressed as CSD code words of n bits (n: natural numbers more than 2), comprising the steps:

creating as a virtual common subexpression common subexpressions created by bit-shift, bit-add, or bit-inversion of random coefficient subexpressions out of the digital filter coefficients, thereafter shifting the digital samples by the number of bits corresponding to the common subexpression and the virtual common subexpression;

adding up all the digital samples shifted by the number of bits corresponding to the common subexpressions to obtain a composite output value of a common coefficient tap line;

obtaining composite output values of random coefficient tap lines by adding up the digital samples shifted by the number of bits corresponding to the virtual common subexpression and the composite output value of the common coefficient tap line being used as a common input; and

performing in order delaying and adding to create filter output values by subsequent compositions of the composite output values of the common coefficient tap lines and the composite output values of the random coefficient tap lines.

8. The method of claim 7, wherein the number of the tap lines is set as 73 in case where the digital filter is used in a middle frequency terminal of a mobile radio communication system.

9. The method of claim 8, wherein the number of bits of the CDS code word is 24 bits.

10. A digital filter, comprising:

a shift register group including first shift register members each receiving digital samples of k bits as input signals and shifting the received digital samples by bit shift values of filter coefficients that are defined as common subexpressions out of filter coefficients that are expressed as code words of n

bits within CSD code, and second shift register members shifting code words of the other filter coefficients that are not defined as the common subexpressions by using the code words of the common subexpressions;

a adder group including first composite members adding up the shifted digital samples that are output from the first shift register members to provide them to common tap lines, and second composite members for adding the shifted digital samples that are output from the second shift register members to the composite outputs of the common tap lines to provide the results to each of corresponding tap lines;

a delay group including a plurality of delayers connected to the tap lines and being connected in series from one another to provide delay to the composite outputs; and

an output adder group including a plurality of adders for adding up the outputs of the delayers and the composite outputs of the tap lines to create digital output signals of k bit(s).

11. An N tap CSD digital filter having filter coefficients that are expressed as CSD codes, comprising:

a shift register group including first shift register members receiving digital samples of a plurality of bits as input signals and shifting the received digital samples by bit shift values of filter coefficients that are defined as common subexpressions out of the filter coefficients, and second shift register members shifting code words of the other filter coefficients that are not defined as the common subexpressions by using the code words of the common subexpressions;

an adder group including first composite members adding up the shifted digital samples that are output from the first shift register members to provide them to common tap lines, and second composite members for adding the shifted digital samples that are output from the second shift register members to the composite outputs of the common tap lines to provide the results to each of the corresponding tap lines;

a delay group including a plurality of delayers connected to the tap lines and being connected in series from one another to provide delay to the composite outputs; and

an output adder group including a plurality of adders for adding up the outputs of the delayers and the composite outputs of the tap lines to create digital output signals of k bit(s).

12. The digital filter of claim11, wherein the common tap line is a tap line of filter coefficients having the greatest number of common coefficient subexpressions out of the filter coefficients.

13. The digital filter of claim 11, wherein the digital filter is designed with software by a digital signal processor performing shifting, adding, and delaying.

14. A method for implementing a digital filter having a plurality of filter coefficients, each expressible as a canonical signed digit code word, the method comprising:

forming a virtual common subexpression that is relevant to a first of the plurality of filter coefficients;

forming at least a second subexpression for at least a second of the plurality of filter coefficients in terms of the virtual common subexpression so that adders are shared with the virtual common subexpression in a tap line of at least the second of the plurality of filter coefficients.

15. A method as defined in Claim 14 wherein at least the second subexpression is formed from the virtual common subexpression through at least one of a bit-shift, a bit-add and a bit-inversion.

16. A method as defined in Claim 14 wherein each of the plurality of filter coefficients is formed from the virtual common subexpression through at least one of a bit-shift, a bit-add and a bit-inversion.

17. A program storage device readable by a machine, tangibly embodying a program of instructions executable by the machine to perform method steps for implementing a digital filter having a plurality of filter coefficients, each coefficient expressible as a canonical signed digit code word, the method steps comprising:

forming a virtual common subexpression that is relevant to a first of the plurality of filter coefficients;

forming at least a second subexpression for at least a second of the plurality of filter coefficients in terms of the virtual common subexpression so that adders are shared with the virtual common subexpression in a tap line of at least the second of the plurality of filter coefficients.

18. A system for implementing a digital filter having a plurality of filter coefficients, each expressible as a canonical signed digit code word, the system comprising:

means for forming a virtual common subexpression that is relevant to a first of the plurality of filter coefficients;

means for forming at least a second subexpression for at least a second of the plurality of filter coefficients in terms of the virtual common subexpression so that adders are shared with the virtual common subexpression in a tap line of at least the second of the plurality of filter coefficients.

19. A digital filter comprising:

at least one shift register for receiving digital samples of input signals and shifting the received digital samples by bit-shift values of filter coefficients that are defined relative to a virtual common subexpression;

a first adder for adding shifted digital samples that are output from the at least one shift register to drive a common tap line;

a second adder for adding shifted digital samples that are output from the at least one shift register to the output of the common tap line to drive a tap line corresponding to a filter coefficient; and

at least one delay unit connected to a tap line for delaying an output signal component.

20. A digital filter comprising:

means for receiving digital samples of input signals;

means for shifting the received digital samples by bit-shift values of filter coefficients that are defined relative to a virtual common subexpression;

means for adding shifted digital samples to drive a common tap line;

means for adding shifted digital samples to the output of the common tap line to drive a tap line corresponding to a filter coefficient; and

means for delaying an output signal component corresponding to a tap line.

21. A program storage device readable by a machine, tangibly embodying a program of instructions executable by the machine to perform method steps for digitally filtering input signals, the method steps comprising:

receiving digital samples of the input signals;

shifting the received digital samples by bit-shift values of filter coefficients that are defined relative to a virtual common subexpression;

adding shifted digital samples to drive a common tap line;

adding shifted digital samples to the output of the common tap line to drive a tap line corresponding to a filter coefficient; and

delaying an output signal component corresponding to at least one of a filter coefficient and a tap line.